library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity RAM is

port(clk,reset,WriteEnable: in std\_logic;

addr: in std\_logic\_vector(3 downto 0);

Data: inout std\_logic\_vector(3 downto 0));

end RAM;

architecture RAM1 of RAM is

type Memory is array (15 downto 0) of std\_logic\_vector(3 downto 0);

signal MemoryMap: Memory;

begin

process(clk,reset)

begin

if Reset = '1' then

for i in 15 downto 0 loop

MemoryMap(i)<="0000";

end loop;

elsif clk='1' and clk'event then

if(WriteEnable = '1') then

MemoryMap(conv\_integer(addr))<= Data;

else

data <= MemoryMap(conv\_integer(addr));

end if;

end if;

end process;

end RAM1;